What is Claimed Is:

1. A semiconductor device having a conduction channel having a width which is electrically modulated comprising:

a substrate including a diffusion region;

a gate disposed over said diffusion region; and

a trench structure formed in said substrate, enclosing said diffusion region, said trench structure modulating a width of a first channel in said diffusion region below said gate, in response to a voltage potential applied between said trench structure and said substrate which is capacitively coupled to said channel.

2. The semiconductor device according to claim 1 wherein said trench structure comprises a trench etched in said substrate and filled with polysilicon, having an oxide liner insulating said trench from said substrate.

3. The semiconductor device according to claim 1 further comprising a plurality of gates over said diffusion region, forming a plurality of channels which are commonly controlled with said first channel by said voltage potential.

4. A semiconductor device for providing first and second matched sets of resistors comprising:

a common substrate including a first and second trench structures enclosing first and second diffusion regions;

a first plurality of resistors in said first diffusion region;

a second plurality of resistors in said second diffusion region; and

first and second control terminals connected to said first and second trench structures for applying first and second control voltages between said trench structures and

said substrate, whereby a channel width of each of said resistors of a plurality of resistors may be controlled.

5. The semiconductor device according to claim 4 further comprising:

a first differential amplifier having an inverting input connected to a source of voltage through a first resistor of said first diffusion region, a non inverting input connected to ground through a second resistor of said first diffusion region, and an output terminal connected to said first control terminal; and

a second differential amplifier having a non inverting input connected to said first differential amplifier inverting input and to a source of voltage through a first resistor of said second diffusion region, an inverting input connected to said first differential amplifier non inverting input and to ground through a second resistor in said second diffusion region, and an output terminal serially connected to said second control terminal.

6. A circuit on each of different areas of said substrate having transistors with matching gains comprising:

a first transistor in each of said different areas, each of said first transistors having a substantially equal area and substantially the same gain, which produces substantially the same current in response to the same voltage conditions supplied to each of said first transistors;

second and third transistors located in a trench in each of said different areas, having substantially the same gain controlled by a voltage applied to said trench, said second transistor being serially connected with said first transistor and having a gate connected to the gate of said first transistor; and

a feedback voltage connected from said first transistor source to said trench, providing a voltage which modulates the channel width of said second and third voltage transistors, and which produces substantially the same current through said first and second

transistors of said different areas, thereby producing substantially the same gain for said third transistors of different areas of said substrate.

7. The circuit according to claim 6 further comprising a current source serially connected with one of said third transistors and a gate of said one third transistor, and a connection between gates of said third transistors which establishes a common current through all of said third transistors.

8. The circuit according to claim 6 wherein said feedback voltage is derived from the serial connection of said first and second transistors.

9. The circuit according to claim 6 wherein said second and third transistors occupy substantially less area than said first transistor.

10. The circuit according to claim 6 wherein said first and second transistor gates are connected to a common source of voltage.

11. A current source for a branch of a digital to analog converter comprising:

a transistor located within a trench structure, said transistor having a gate connection connected to a source of gate voltage, and a source and drain connected to supply a current to first and second transistors, one of which supplies current to an output terminal, the other of which diverts current from said output terminal, in response to a respective first and second state of a digital data bit; and

means for supplying a bias voltage to said trench to modulate the effective width of said transistor in said trench structure whereby said current diverted to said output terminal may be set with respect to other branches of said digital to analog converter.

12. The current source for a branch of a digital to analog converter according to claim 11 wherein said means for supplying a bias voltage is a bias circuit which may be trimmed to provide a bias voltage which will set the current level for said branch.

13. In a digital to analog converter circuit which produces a voltage proportional to an input digital signal, a voltage to current converter circuit comprising:

at least one transistor in a trench isolation structure, having drain source connections connected between a source of voltage and a common output terminal, and a gate terminal connected to a source of bias voltage; and

said trench structure receiving said digital to analog voltage proportional to said input digital signal, said voltage modulating a channel width of said transistor, whereby an output current is produced by said common output terminal representing said input digital signal.

14. The voltage to current converter according to claim 13 comprising a second transistor in said trench structure connected in parallel with said one transistor.

15. An IC chip comprising:

a substrate;

a plurality of devices formed in the substrate and each including a channel for conducting current, the channel having a length and a width;

a plurality of voltage terminals for providing a controllable voltage level; and

a plurality of conductive regions formed in the substrate and each connected to one of the voltage terminals, wherein the conductive regions are each formed sufficiently nearby at least one of the channels such that a voltage level of the conductive region modulates the width of said at least one of the nearby channels in response to a voltage level provided to the conductive region by said one of the voltage terminals.

16. The chip of claim 15, wherein the plurality of devices are FETs each having diffusion regions formed in the substrate at two ends of the length of its channel and each having a gate formed above its channel.

17. The chip of claim 15, wherein the plurality of devices are resistors each having terminals formed in the substrate at two ends of the length of its channel.

18. The chip of claim 15, wherein the channel is insulated from its nearby conductive region by an insulative material.

19. The chip of claim 18, wherein the nearby conductive region surrounds the channel.

20. A method for making a semiconductor chip comprising:

forming a diffusion region in a semiconductor substrate;

forming an insulated trench structure in said substrate which surrounds said diffusion region; and

forming electrical connections on said trench structure and said substrate which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region.

21. The method for making a semiconductor chip according to claim 20, further comprising source and drain regions formed in said diffusion region on each side of said gate.

22. The method for making a semiconductor chip according to claim 20, wherein said diffusion region forms a resistor which has a resistance controlled in response to said control voltage.

23. The method for making a semiconductor chip according to claim 20, wherein said diffusion layer is formed in a well of polysilicon deposited in said trench structure.

24. A method for making a semiconductor chip comprising:

forming first and second diffusion regions in a semiconductor substrate;

forming a trench structure around said first and second diffusion regions; and

forming a contact on said trench structure and said substrate for controlling current through said diffusion regions.

25. The method for making a semiconductor chip according to claim 24, further comprising:

forming first and second gates over said first and second diffusion regions.

26. A method for making a semiconductor chip comprising:

forming multiple trench structures on a substrate;

forming multiple diffusion regions in said trench structures in said substrate; and

forming multiple contacts on each of said trench structures and said substrate for controlling current through said diffusion regions.

27. The method for making a semiconductor chip according to claim 26, further comprising:

forming a gate electrode over each of said diffusion regions; and

forming drain and source connections on opposite sides of said gate electrodes.